IN THE CLAIMS:

Please amend the claims set forth below.

1. (Original) A memory device capable of controlling a characteristic parameter, comprising:

a register controller comprising a nonvolatile memory unit for storing data in the nonvolatile memory unit; and

a parameter controller configured to output a signal having a characteristic parameter depending on a signal outputted from the register controller.

2. (Original) The memory device according to claim 1, wherein the register controller comprises:

a register array comprising a plurality of registers; and

a register command processor configured to receive a plurality of signals, to identify a mode as a program mode or a read mode by decoding the plurality of signals, and individually control the plurality of registers according to the identified mode.

3. (Original) The memory device according to claim 2, wherein each of the plurality of registers comprises:

a first amplifier configured to amplify and maintain a voltage of a first node having a higher potential between a second node and a third node, at a positive voltage in response to a first control signal;

a second amplifier configured to amplify and maintain a voltage of a fourth node having a lower potential between the second node and the third node, at ground voltage in response to a second control signal;

an input unit configured to provide a data signal to the second node and the third node in response to a third control signal; and

a storage unit configured to store the data signal provided to the second node and the third node in response to a fourth signal, wherein the data signal remains stored while a power to the memory device is off.

4. (Original) The memory device according to claim 3, wherein the first amplifier comprises:

a first PMOS transistor comprising a gate connected to receive the first control signal and a source connected to a positive power source;

a second PMOS transistor comprising a gate connected to the first node, a source connected to a drain of the first PMOS transistor, and a drain connected to the third node; and

a third PMOS transistor comprising a gate connected to the third node, a source connected to the drain of the first PMOS transistor, and a drain connected to the second node.

5. (Original) The memory device according to claim 3, wherein the second amplifier comprises:

a first NMOS transistor comprising a gate connected to the second node and a drain connected to the third node;

a second NMOS transistor comprising a gate connected to the third node and a drain connected to the second node; and

a third NMOS transistor comprising a gate connected to receive the second control signal, a drain connected to a source of the first NMOS transistor and a source of the second NMOS transistor, and a source connected to ground.

6. (Original) The memory device according to claim 3, wherein the input unit comprises:

a first NMOS transistor comprising a gate connected to receive the third control signal, a source connected to receive a first data signal, and a drain connected to the second node; and

a second NMOS transistor comprising a gate connected to receive the third control signal, a source connected to receive a second data signal, and a drain connected to the third node.

7. (Original) The memory device according to claim 3, wherein the storage unit comprises:

a first ferroelectric capacitor comprising a first terminal connected to receive the fourth control signal, and a second terminal connected to the second node;

a second ferroelectric capacitor comprising a first terminal connected to receive the fourth control signal, and a second terminal connected to the third node;

a third ferroelectric capacitor comprising a first terminal connected to the second node, and a second terminal connected to ground; and

a fourth ferroelectric capacitor having a first terminal connected to the third node, and a second terminal connected to ground.

8. (Original) The memory device according to claim 2, wherein the register command processor is configured to start a program mode if an output enable signal toggles a predetermined number of times while a write enable signal and a chip enable signal included in the received plurality of signals are activated, and not respond to the write enable signal, the chip enable signal and the output enable signal during the program mode.

9. (Original) The memory device according to claim 1, wherein the memory device is a ferroelectric memory device.

10. (Original) The memory device according to claim 9, wherein the ferroelectric memory device comprises:

a plurality of unit cells;

a plurality of switches; and

bitlines comprising sub bitlines connected to the plurality of unit cells and a main bitline connected to the plurality of sub bitlines via the plurality of switches,

wherein the plurality of switches is configured so that when a predetermined unit cell of the plurality of unit cells is accessed, only a switch for connecting a particular one of the plurality of sub bitlines connecting the predetermined unit cell to the main bitline is turned on, and other switches for connecting the rest of the plurality of sub bitlines to the main bitline are all turned off.

11. (Original) A memory device capable of controlling a characteristic parameter, comprising:

a register controller comprising a nonvolatile memory unit configured to store data;

a current controller configured to output an amount of current that is controlled according to a signal outputted from the register controller;

a signal processor configured to receiving an external signal, and change and output a voltage level of the received external signal according to the amount of current outputted from the current controller; and

a buffer configured to receive a signal outputted from the signal processor.

12. (Original) The memory device according to claim 11, wherein the external signal received by the signal processor is one of an address signal, a data signal and a control signal.

13. (Original) The memory device according to claim 11, wherein the signal processor further comprises a voltage fixing means for receiving a control signal, and fixing a signal outputted from the signal processor at a predetermined voltage level regardless of the external signal when the control signal is inactivated.

14. (Original) A memory device including a parameter controlling capability, comprising:

a register controller comprising a nonvolatile memory unit;

a current controller configured to control an amount of current according to a signal outputted from the register controller;

a capacitor connected between an output terminal of the current controller and ground; and

a delay controller configured to delay an externally inputted signal for a predetermined time according to the amount of current outputted from the current controller and a capacitance of the capacitor, and output the delayed signal.

15. (Original) A memory device capable of controlling a characteristic parameter, comprising:

a register controller comprising a nonvolatile memory unit and configured to output a plurality of signals;

a current controller configured to control an amount of current outputted according to the plurality of signals outputted from the register controller; and

a delay controller configured to delay an externally inputted signal for a predetermined time according to the amount of current outputted from the current controller and a capacitance of a capacitor connected between an output terminal and a ground, and output the delayed signal.

16. (Original) A memory device capable of controlling a characteristic parameter, comprising:

a register controller comprising a nonvolatile memory unit and configured to output a plurality of signals;

a current controller configured to control an amount of current outputted according to the plurality of signals outputted from the register controller;

a current fixer comprising a first end and a second end and configured to fix an amount of current flowing through both ends; and

a voltage generator connected between the current controller and the current fixer, and configured to output a predetermined voltage according to an externally inputted control signal, the amount of current outputted from the current controller, and the amount of current flowing through the current fixer.

17. (Original) The memory device according to claim 15, wherein the current controller comprises a plurality of PMOS transistors each comprising a gate, a drain and a source, wherein for each of the plurality of PMOS transistors the gate is connected to receive one of the plurality of signals outputted from the register controller, the source is connected to a common positive power source, and the drain is connected to a common current output.

18. (Original) The memory device according to claim 16, wherein the current controller comprises a plurality of PMOS transistors each comprising a gate, a drain and a source, wherein for each of the plurality of PMOS transistors the gate is connected to receive one of the plurality of signals outputted from the register controller, the source is connected to a common positive power source, and the drain is connected to a common current output.

19. (Original) An integrated circuit device capable of receiving an input signal and generating an output signal having signal performance characteristics, comprising:

a signal performance characteristic controller configured to control one or more of the signal performance characteristics of the integrated circuit device.

20. (Currently amended) An integrated circuit device according to ~~claim 23~~ claim 19, wherein the signal performance characteristic controller comprises:

a register controller configured to provide a plurality of control signals;

a plurality of registers each coupled to the register controller to receive as an input at least one of the plurality of control signals and configured to generate, in response to the at least one control signal, a register output signal as an output; and

a plurality of transistors each comprising a source coupled to a voltage source, a gate configured to receive the register output signal of at least one of the plurality of registers, and a drain, wherein each of the drains of two or more of the plurality of transistors are coupled to provide a common output,

wherein the common output controls the signal performance characteristic of the integrated circuit device.